Getting data where it's needed
potential for CPU, GPU, accelerators, and smart networks

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Agenda

1. Motivation and Data Processing Unit (DPU) definition

2. Use cases

3. DPU requirements

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Motivation

- Network scale-out challenges – Frontier/LUMI

- Very tight integration/coupling

- Good for weak scaling, but worse for strong scaling

- Latency and bandwidth both major players

- Irregular network requirements
  - Inherent imbalance
  - Each rank with different problem sizes or workload
  - Workflows with different coupled apps

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Data Processing Unit (DPU) definition

- DPU as a new type of accelerator or integration/coupling of different accelerators?

- Definition
  - Controlling data streaming and collective processing
  - Managing network traffic, protocols and storage
  - Abstraction of a DPU as a collection of devices

- Requirements clash and overlap: cloud vs. traditional HPC
  - Opportunities: what needs prioritizing for these different kinds of deployments
    - Cloud prioritizes data confidentiality and tenant isolation
    - HPC prioritizes low latencies
    - Both prioritize core count – more cores maps to more revenue (cloud) and performance (HPC)
  - Convergence of technologies: create technology that is transferable across HPC and cloud
    - Widespread modelling and simulation offerings
    - Deep learning frameworks
  - Variety of workloads in HPC which might be different from what is in the cloud
    - ML workloads showcasing different requirements than HPC apps
    - Requirement shift depending on the scale

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Good use cases for DPUs

- Sparse Machine Learning communication challenges over the network
- Serialization/deserialization of data
- RDMA and shared memory abstractions for a collection of nodes
- Enabler for composability of resources
- High-performance distributed storage
- Offloading programming models (e.g., collectives or other distributed operations)
- Data-lake enabler
- Be smarter behind existing APIs
  - Evolve standards to accommodate user needs and HW limitations
  - Can we keep/simplify the same API and be smarter in their implementation?
    - Examples: MPI, RCCL/NCCL

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Co-design across different classes of hardware

- Convergence of multiple flavors of technology
  - CPUs
  - GPUs
  - FPGAs
  - SW defined networks
  - Offloading model applied everywhere
  - From components to systems
  - From systems to a user abstraction
  - Co-design
    - with system integrator
    - Within the SoC
    - Across a network
    - Toolchains – software libraries and tooling

Co-design

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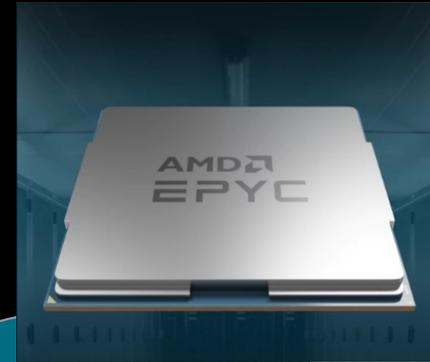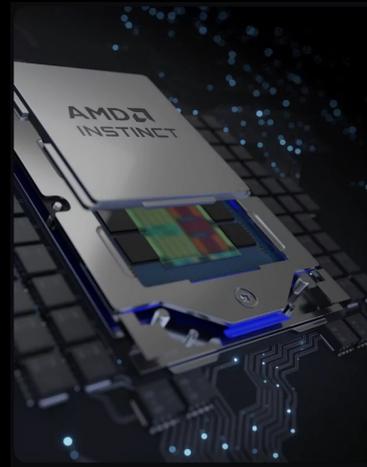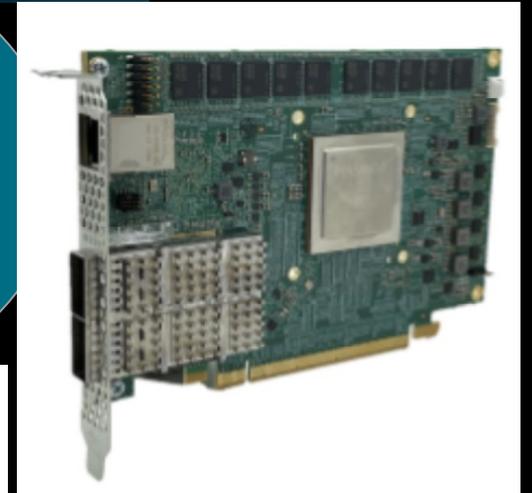
What's happening around the GPUs

- CPU+GPU unification – MI300 APU
  - Keep data in the same place – move the compute
  - Abstraction lifts the need for user-defined copies
  - Can we expand the abstraction beyond the APU?

AMD CDNA™ 2 Coherent Memory Architecture ➤ AMD CDNA™ 3 Unified Memory APU Architecture

- **Simplifies Programming**

- **Low Overhead 3rd Gen Infinity Interconnect**

- **Modular System Design**

CPU   GPU

CPU Memory (DDR)

GPU Memory (HBM)
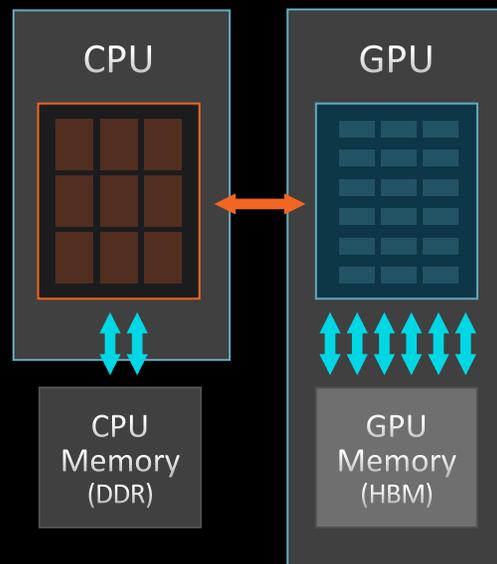
- **Eliminates Redundant Memory Copies**

- **High-Efficiency 4th Gen AMD Infinity Architecture**

- **Low TCO with Unified Memory APU Package**

Next-Gen AMD Instinct™ APU

Unified Memory (HBM)

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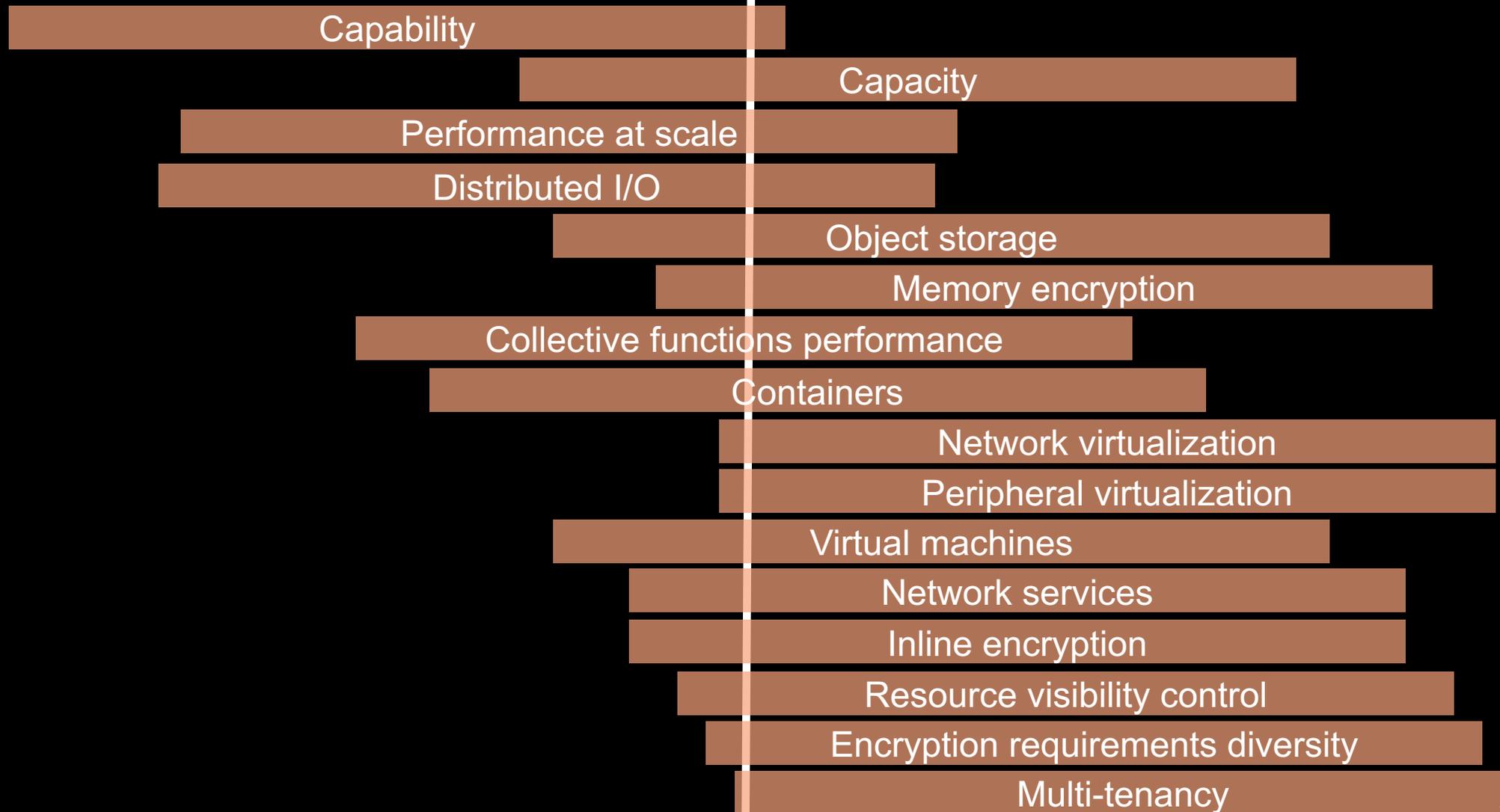
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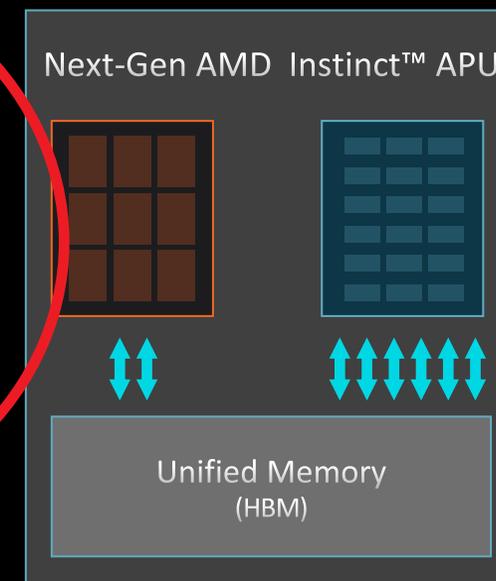
A global shared memory abstraction

- Reflective memory

- Stop thinking about nodes but a collection of resources

- Composability of resources

- The enablers
  - RDMA around compute units
  - Flexible/adaptable (SW defined) network
  - Smart NICs – configurable data processors

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HPC/Cloud requirements/priorities

On-premise HPC   Cloud

Capability

Capacity

Performance at scale

Distributed I/O

Object storage

Memory encryption

Collective functions performance

Containers

Network virtualization

Peripheral virtualization

Virtual machines

Network services

Inline encryption

Resource visibility control

Encryption requirements diversity

Multi-tenancy

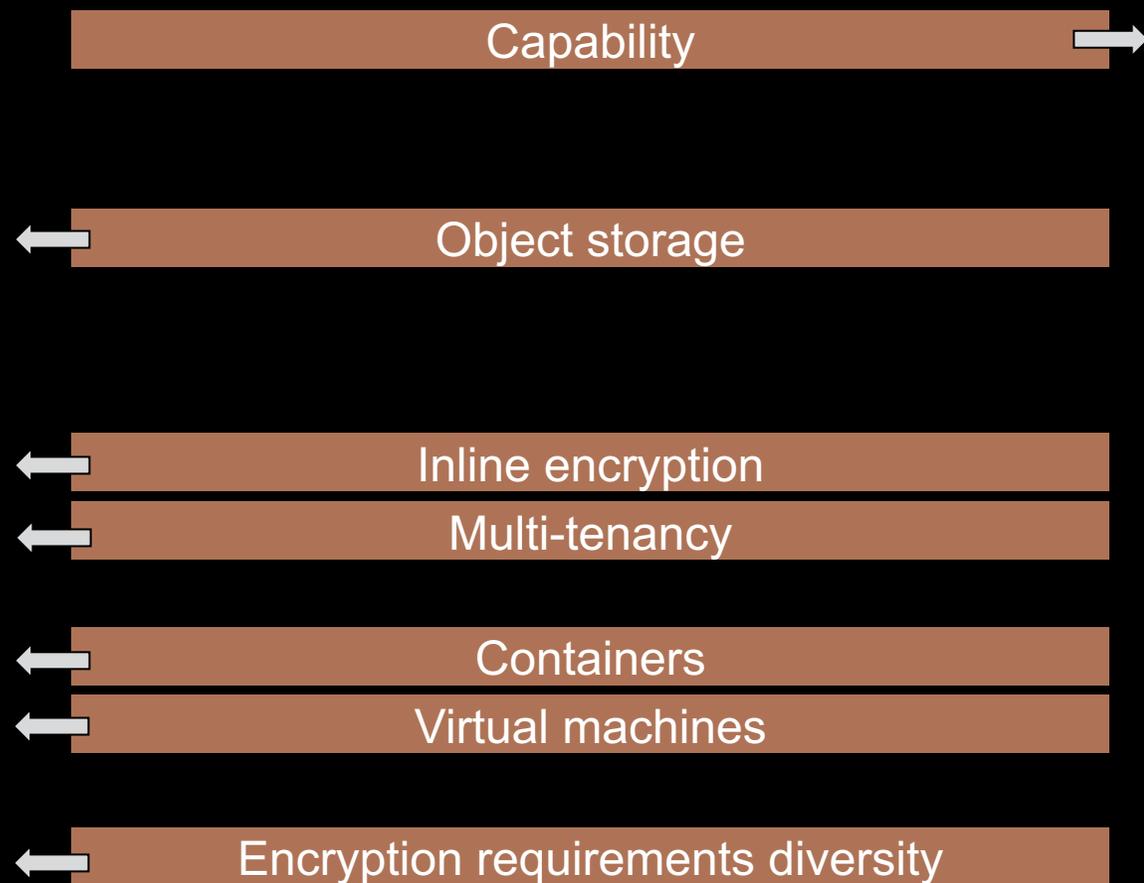25 May 2023

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How are these bars moving?

- More capability runs attempted on the cloud
  - Distributed deep learning
  - Modeling and simulation offerings
- Object storage implementations in-house
  - Data organization beyond the file abstraction
  - Extra metadata annotations
  - Data streaming from object store services
- Sensitive data used everywhere
  - General Data Protection Regulation – GDPR
  - Data quality as competitive advantage
  - Encryption desired in many workloads
- Containers and other sort visualization first class citizens
  - Most HPC sites support container engines
  - Dodge native filesystem – in-memory overlay file system
- Flexible deployments
  - No static/immutable functions
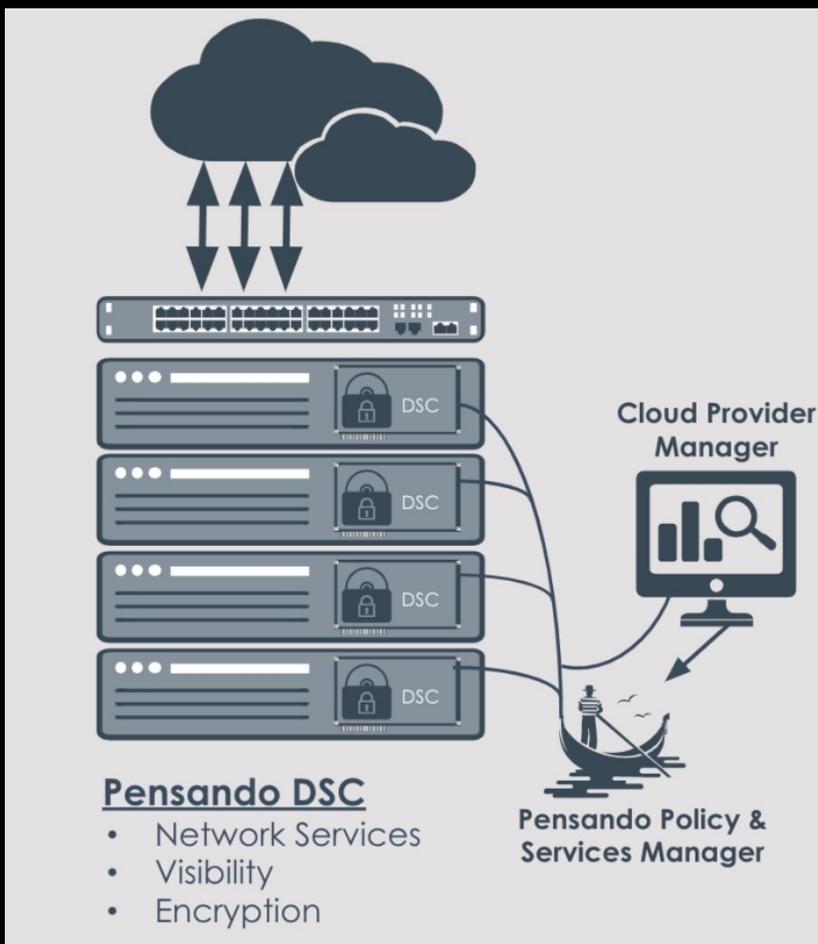 - Accommodate new standards and workloads

On-premise HPC   Cloud

Capability

Object storage

Inline encryption

Multi-tenancy

Containers

Virtual machines

Encryption requirements diversity

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DPUs and Smart NICs – complementing capabilities

Distributed Services Card (DSC)

AMD SmartNIC Accelerator

Pensando DSC
- Network Services
- Visibility
- Encryption

Cloud Provider Manager

Pensando Policy & Services Manager

Highly manageable and fully programmable

Complete function set tightly coupled with programmable logic (up to 400G)

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Pensando DSC

Centrally Managed	Policy	Automation	Observability	Ecosystem
Policy & Services Manager	Orchestration & Provisioning	REST API	Troubleshooting & Security	Compute, Analytics, IT Ops

Stateful Firewall · Encryption & TLS Offload · Micro Segmentation · Load Balancer · Networking · Storage Services

Telemetry

Pensando Distributed Services Cards

DSC · DSC · DSC · DSC · DSC · DSC · DSC · DSC · DSC

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FPGA Smart NICs structure

PCIe

Interconnect

Host Subsystem
(CPM5N)

Network Subsystem
(HNICX)

Programmable Network on Chip

Programmable
Logic

Processing Subsystem
(PSX)

Memory Subsystem

Programmable Network on Chip

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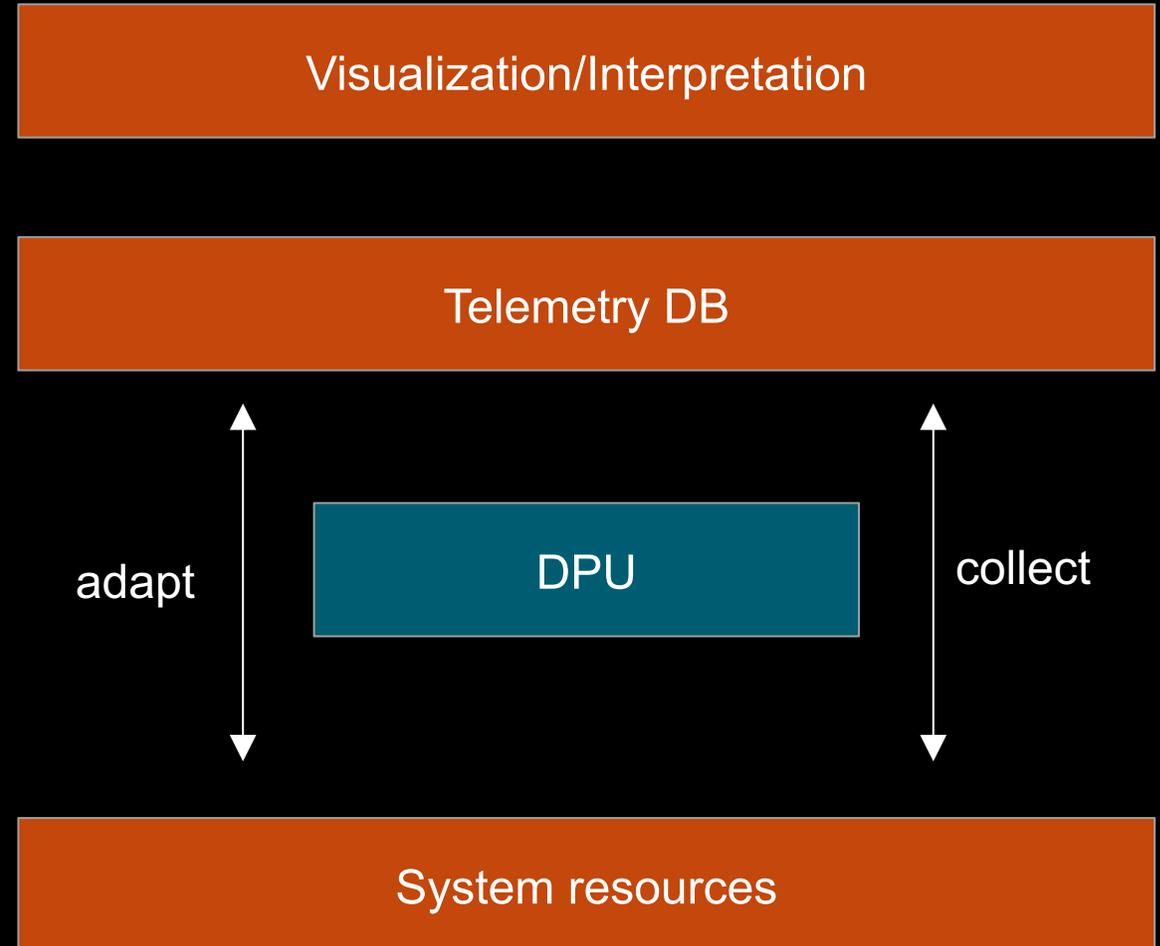together we advance_
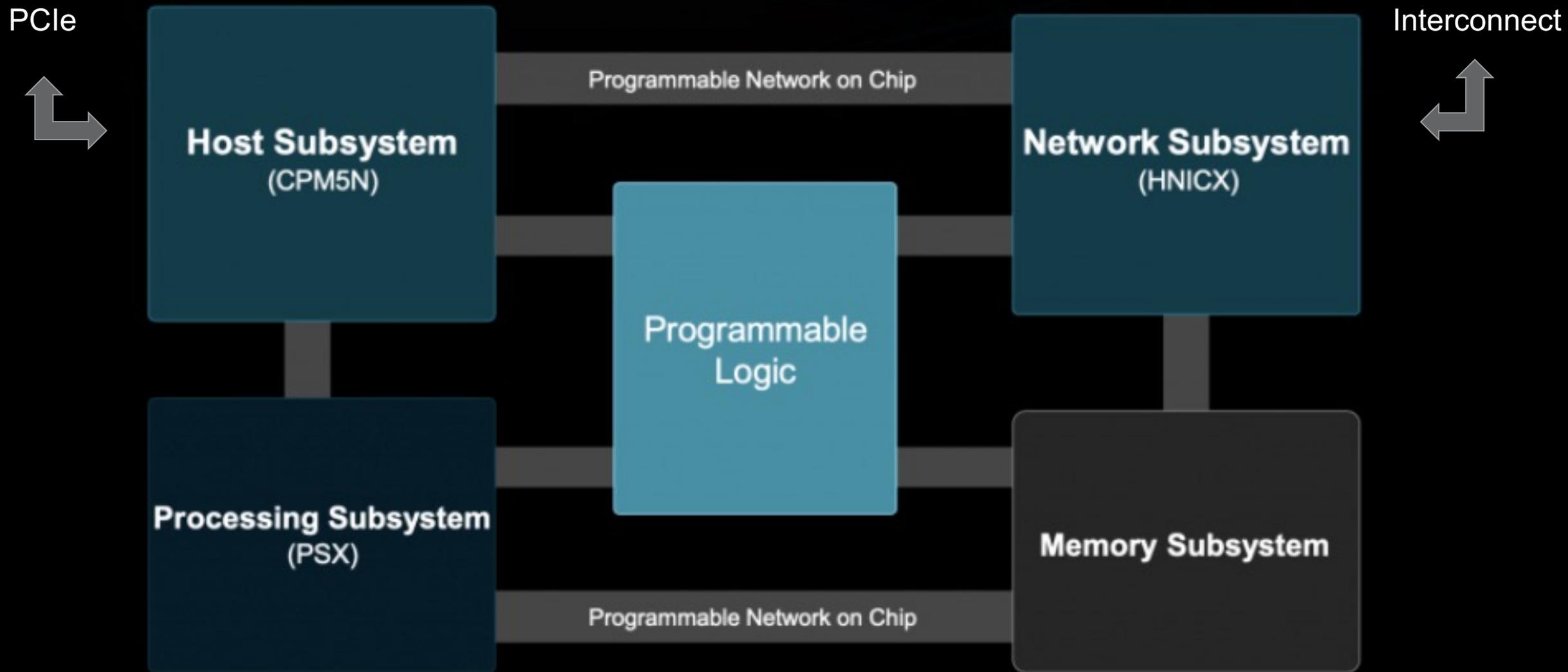
Programmability across all devices

- Bespoke solutions
  - Accommodate diversity of use cases
- Ease of use
  - User-friendly abstractions
  - Enable developers and end users
  - Facilitate training and knowledge transfer
- Evolve solutions over time
  - New security standards
  - New communications patterns
  - Address lessons learned
- AMD DPUs support
  - P4 packet domain specific language
  - C programming languages
- FPGA
  - Feature rich high-level-synthesis tooling
  - Many ready-to-deploy configurable IP instances

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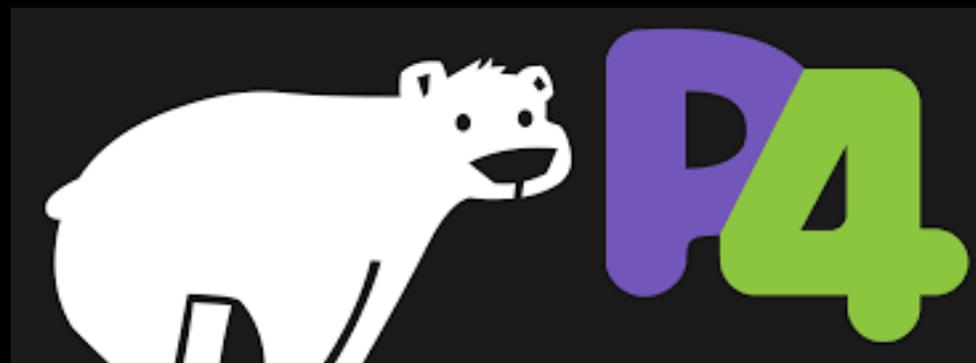
Tooling and telemetry

- Performance is hard to assess
  - Collect data seamlessly
  - No workload disruption
  - Minimum user intervention
  - Low overhead performance sampling
- Integrate with popular profiling tools
- Visualization of traces
  - Realtime view
- Find what is actionable
  - How far off from peak empirical performance
  - Self calibration
- Translate findings into the network configuration
- Telemetry for different workloads
  - Learn what is latency bound
  - Learn what is bandwidth bound
  - Learn when to save power
    - Link cooling down

Visualization/Interpretation

Telemetry DB

adapt   DPU   collect

System resources

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Making smarter APIs

- Users (would) love
  - Stick with legacy APIs
  - Have simple and high-level application-level API
  - Ignore hardware intricacies
  - Simple abstractions
  - Focus on their science
- API developers (would) love
  - Digest all possible application-level information
  - Offload parameterization to the user
  - Have the user pick sensible defaults
- Can we meet in between?
- DPUs to make API implementation smarter
  - Collect telemetry
  - Realize sub-optimal decisions
  - Tune on-the-fly
  - Maintain data-base of good practices
  - Identify application signatures and map it to better defaults

Users/Developers

API

DPU

Smart decisions

System resources

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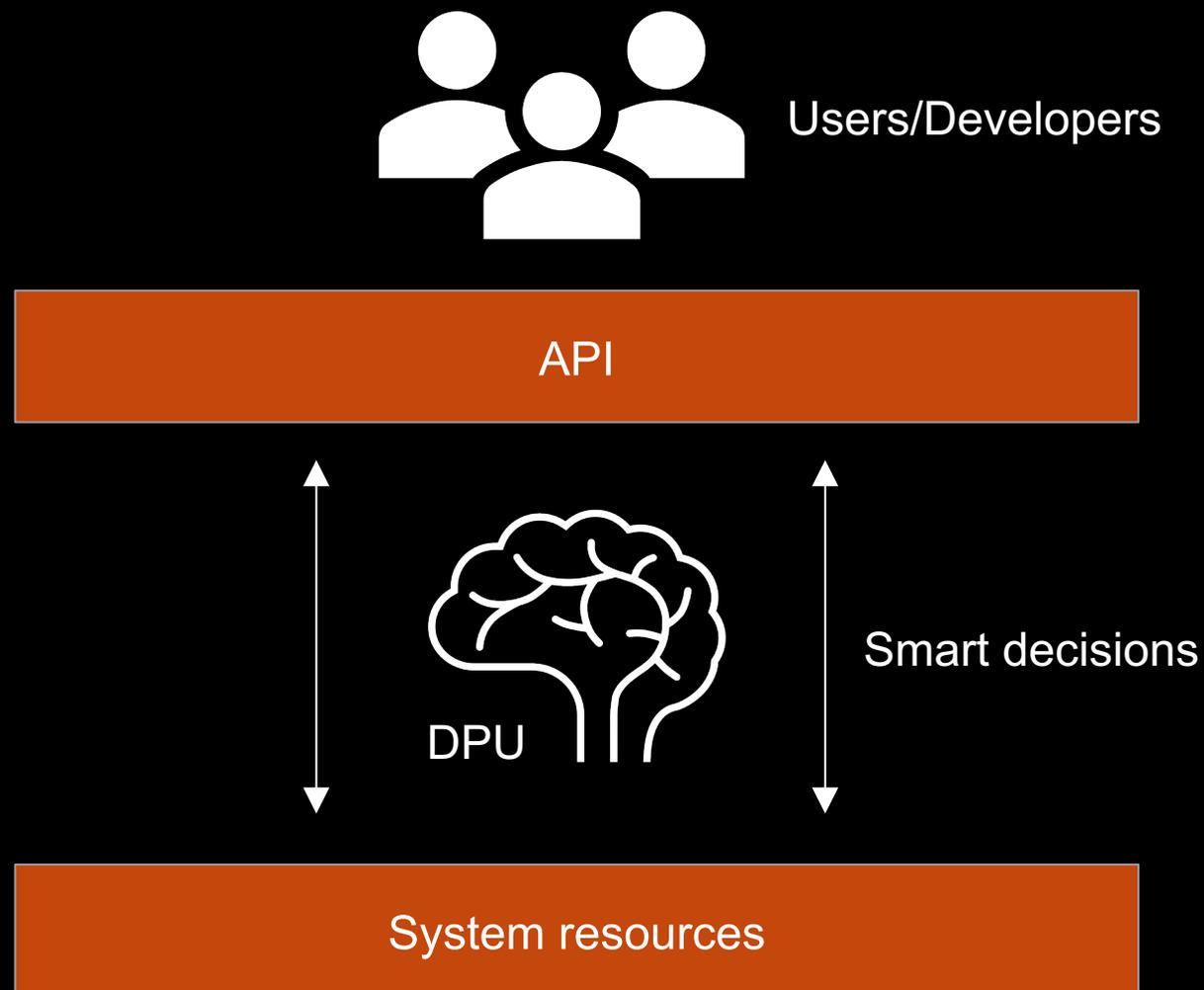
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